

II. IN THE CLAIMS

1. (previously amended) In a ROM device using a plurality of data resistors to interconnect a plurality of input word lines with a plurality of output bit lines, a temperature compensation circuit to maintain a current through a selected one of a plurality of data resistors substantially constant comprising:

- at least one reference resistor, wherein the conductivity of said reference resistors is responsive to changes in temperature;
- a constant current source coupled to said at least one reference resistor, said constant current source developing a voltage across said at least one reference resistor; and
- at least one switch connected to said at least one reference resistor to selectively couple said voltage to a plurality of input word lines wherein the ROM device uses said plurality of data resistors to interconnect said plurality of input word lines with a plurality of output bit lines.

2. (previously amended) A temperature compensation circuit as recited in Claim 1 wherein electrical conductive properties of said reference resistor are selected to be the same as the electrical conductive properties of said data resistors.

3. (original) A temperature compensation circuit as recited in Claim 2 wherein said data resistor is selected from a polysilicon material.

4. (original) A temperature compensation circuit as recited in Claim 3 wherein said polysilicon material is undoped.

1 5. (original) A temperature compensation circuit as recited in Claim 3 wherein said
2 polysilicon material is doped.

1 6. (original) A temperature compensation circuit as recited in Claim 2 wherein said
2 data resistor is comprised of a metal oxide.

1 7. (previously amended) A temperature compensation circuit as recited in Claim 1
2 wherein conductive properties of said reference resistors are selected such that a
3 change in electrical conductive properties of said reference resistors matches a
4 change in electrical conductive properties of said data resistors.

1 8. (original) A temperature compensation circuit as recited in Claim 7 wherein said
2 data resistor is selected from a polysilicon material.

1 9. (original) A temperature compensation circuit as recited in Claim 8 wherein said
2 polysilicon material is undoped.

1 10. (original) A temperature compensation circuit as recited in Claim 8 wherein said
2 polysilicon material is doped.

1 11. (original) A temperature compensation circuit as recited in Claim 7 wherein said
2 data resistor is comprised of a metal oxide.

1 12. (original) A temperature compensation circuit as recited in Claim 1 further
2 comprising:
3 a plurality of sense amplifiers coupled to said output bit lines, each output
4 line having at least one sense amplifier, said sense amplifier receiving said

5 constant current flowing through said data resistors wherein each of said sense
6 amplifier provides a constant output voltage.

1 13. (original) A temperature compensation circuit as recited in Claim 12 wherein said
2 sense amplifier comprises
3 an operational amplifier with a fixed feedback resistor, R, wherein said
4 amplifier output voltage is determined from the value of said constant current and
5 said feedback resistor.

1 14. (original) A temperature compensation circuit as recited in Claim 13 wherein said
2 feedback resistor is temperature independent.

1 15. (original) A temperature compensation circuit as recited in Claim 1 wherein said at
2 least one switch selectively couples said voltage to a selected one of said input
3 word lines when an input to said switch is high.

1 16. (original) A temperature compensation circuit as recited in Claim 1 wherein said at
2 least one switch selectively couples said voltage to a selected one of said input
3 word lines when an input to said switch is low.

1 17. (original) A temperature compensation circuit as recited in Claim 12 wherein said
2 sense amplifier is operated in the non-linear region.

1 18. (original) A temperature compensation circuit as recited in Claim 12 wherein said
2 sense amplifier is operated in the linear region.

1 19. (currently amended) A method to maintain a current through Read-Only
2 Memory (ROM) substantially constant as temperature changes comprising the
3 steps of:
4 selecting a reference resistor wherein said ROM employs a plurality of
5 data resistors to provide electrical interconnections between a plurality of input
6 lines and output lines and a change in electrical conductive properties of said
7 reference resistor matches a change in electrical conductive properties of said data
8 resistor;
9 supplying a reference voltage to said input lines, said reference voltage
10 developed by supplying a constant current to said reference resistor, wherein said
11 reference voltage is responsive to a change in temperature and selectively
12 switching said reference voltage to said word line.

1 20. (original) The method as recited in Claim 19 wherein said data resistor is comprised
2 of undoped polysilicon.

1 21. (original) The method as recited in Claim 19 wherein said data resistor is comprised
2 of doped polysilicon.

1 Cancel claim 22.

1 23. (previously amended) In a ROM device, a temperature compensation circuit to
2 maintain a current through a selected one of a plurality of data resistors
3 substantially constant comprising:

4 at least one voltage source producing a voltage that is responsive to
5 changes in temperature; and
6 at least one switch connected to said at least one voltage source to
7 selectively couple said voltage to a plurality of input word lines wherein the ROM
8 device uses said plurality of data resistors to interconnect said plurality of input
9 word lines with a plurality of output bit lines.

1 24. (original) A temperature compensation circuit as recited in Claim 23 further
2 comprising:

3 a plurality of sense amplifiers coupled to said output bit lines, each output
4 line having at least one sense amplifier, said sense amplifier receiving said
5 constant current flowing through said data resistors wherein each of said sense
6 amplifier provides a constant output voltage.

1 25. (original) A temperature compensation circuit as recited in Claim 24 wherein said
2 sense amplifier comprises

3 an operational amplifier with a fixed feedback resistor, R, wherein said
4 amplifier output voltage is determined from the value of said constant current and
5 said feedback resistor.

1 26. (original) A temperature compensation circuit as recited in Claim 25 wherein said
2 feedback resistor is temperature independent.

1 27. (original) A temperature compensation circuit as recited in Claim 24 wherein said
2 sense amplifier is operated in the non-linear region.

1 28. (original) A temperature compensation circuit as recited in Claim 24 wherein said
2 sense amplifier is operated in the linear region.

1 29. (original) A temperature compensation circuit as recited in Claim 23 wherein said at
2 least one switch selectively couples said voltage to a selected one of said input
3 word lines when an input to said switch is high.

1 30. (original) A temperature compensation circuit as recited in Claim 23 wherein said at
2 least one switch selectively couples said voltage to a selected one of said input
3 word lines when an input to said switch is low.

1 31. (original) A temperature compensation circuit as recited in claim 23 wherein said
2 temperature responsive voltage changes to compensate for changes in voltage
3 across said data resistor.

1 32. (currently amended) A method to maintain a current through Read-Only
2 Memory (ROM) substantially constant as temperature changes, comprising the
3 steps of:
4 supplying a reference voltage that is responsive to changes in temperature
5 to a plurality of input lines, wherein said ROM employs a plurality of data
6 resistors to provide electrical interconnections between said plurality of input
7 lines and a plurality of output lines and said reference voltage changes to maintain
8 said current through said data resistor substantially constant and selectively
9 switching said reference voltage to said word line.

1 Cancel claim 33.